ANNUAL LETTER REPORT FOR
RELIABILITY MANAGEMENT THROUGH SELF-TESTING
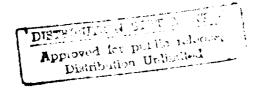
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88

OBJECTIVE

The objective of this project is to develop and study techniques for computational systems with very high degree of readiness. We will study optimal methods of implementing self-testing to achieve this. The topics under examination include fault modeling at different levels, statistical evaluation of self-testing and optimization of self-testing as implemented in hardware and as a background task.

RELEVANCE TO SDI MISSION

The (SDI) will be a critical defensive system. Its major capabilities will be needed for handling only a few rare and unexpected events. The system must not be allowed to fail during these short but extremely critical periods. This requires a very high degree of readiness. We are examining techniques that will allow a very thorough self-check without excessive hardware or performance overheads.

APPROACH

In this project we had started by looking at failures at a low level, i.e. transition level. We have looked at fault modeling, testing and testable design.

In the current phase of the project, we are examining testing of higher level building blocks. These building blocks include register-level components like registers, the combinational logic sandwiched between registers etc. The structural information to be used is also at the register level. The self-test techniques applicable are

1

software/microcode-aided self-test, pseudo random testing and information compression (BIST), and concurrent testing. The self-test strategy must be optimized to keep hardware and performance overheads within acceptable limits.

We have also started examination of statistical techniques to characterize the techniques involved. We would attempt to keep these techniques to be general so that a wide range of self-testing and reliability management schemes can be evaluated.

TECHNICAL PROGRESS

1. Parallelism to Enhance PLA Test Speed:

A new PLA design [5] has been presented which may be easily partitioned into two parts. Both parts may be tested independently and in parallel, thus cutting the test time requirement to about half. The test set is minimal and universal, hence no test generation is required.

2. Single-Pattern Stuck-Open CMOS:

The stuck-open faults in CMOS require two or multi-pattern test-sequences. The available augmentation techniques may fail in presence of glitches [6]. The proposed scheme uses additional transistors to convert a CMOS gate into pseudo-nMOS or pseudo-pMOS during testing. The proposed scheme ensures detection of stuck-open faults in presence of skews/delays, charge sharing or skews. Only a single test pattern per test is required.

2

3. A Testable Two-Dimensional RMC Array:

A testable two-dimensional RMC array design has been presented [9]. Both stuck-at and bridging faults are considered. The augmentation needed is independent of the function implemented. Masking of detectable faults by undetectable faults has also been considered.

4. A Testable RISC-to-CISC Control Architecture:

This investigation addresses testability not at the usual gate level, but at the register level. A new control architecture is presented which is highly testable at the register level [7]. This design uses assignable storage blocks which can be assigned either to the control port or the data port of the processor. The processor can be statically or dynamically reconfigured. Both RISC (small instruction set, large on-chip storage) and CISC (large instruction set, limited on-chip storage) configurations can be achieved. All storage blocks are easily tested. Testability of other parts is under investigation.

REPORTS AND PUBLICATIONS

A. Published:

1. R. Rajsuman, Y.K. Malaiya and A.P. Rajsumana, "On Accuracy of Switch-Level Modeling of Bridging Faults in Complex Gates," Proc. 24th ACM/IEEE Design Automation Conference, June 1987, pp. 244-250.

2. R. Rajsuman, A.P., Jayasumana and Y.K. Malaiya, "On Testing of Complex Gates," Electronic Letters, Vol. 23, No. 16, July 30, 1987, pp. 813-814.

3. B. Gupta, Y.K. Malaiya, Y. Min and R. Rajsuman, "CMOS Combinational Circuit Design for Stuck-Open/Stuck-Short Testability," Proc. Int. Symp. on Ele. Dev., Circ. and Sys., Dec. 1987.

4. R. Rajsuman, A.P. Jayasumana and Y.K. Malaiya, "Testability Analysis for Bridging Faults in Dynamic CMOS," Proc. Int. Symp. on Ele. Dev. Cir. and Sys., Dec. 1987.

B. Technical Reports:

5. R. Rajsuman, Y.K. Malaiya and A.P. Jayasumana, "Parallelism to Reduce PLA Test Time," submitted for publication to IEEE Trans. Ind. Elec.

6. R. Rajsuman, A.P. Jayasumana and Y.K. Malaiya, "CMOS Stuck-open Fault Detection Using Single Test Patterns," submitted for publication to Int. Test Conference.

7. Y.K. Malaiya, "A Testable, Flexible RISC-to-CISC Control Architecture," to be presented at 11th Annual IEEE Workshop on DFT, April 1988.

8. Y.K. Malaiya and P. Verma, "Testability Profile Approach to Software Reliability," Technical Report, in preparation for publication.

9. B. Gupta, B. Bhattacharya, G. Basu, Y.K. Malaiya and R. Rajsuman, "Logical Modeling of Physical Failures and Universal Test Sets in Two Dimensional Cellular Arrays," Technical Report, in preparation for publication.

C. <u>Previous Work in Progress:</u>

10. Y. Min, Y.K. Malaiya and B. Gupta, "On the Computational Complexity of Test Generation for ETG PLAs," in review, <u>IEE Proc. E.</u>

11. Y. Min and Y.K. Malaiya, "Enhancing Detection Capability of Parallel Signature Analyzers," under revision.

12. R. Rajsuman, Y.K. Malaiya and A.P. Jayasumana, "Limitations of Switch Level Analysis for Bridging Faults," under revision.

13. B. Gupta, Y.K. Malaiya, Y. Min and R. Rajsuman, "On Designing Robust Testable CMOS Combinational Circuits," submitted for publication to <u>IEE Proc. E.</u>

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